214443 : DIGITAL ELECTRONICS AND LOGIC DESIGN

Teaching Scheme:	Credits	Examination Scheme:
Lectures: 4 Hours/Week	04	In-Semester (Online): 50 Marks End-Semester: 50 Marks

Prerequisites : Basic Electronics Engineering

Course Objectives :

1. To learn and understand basic digital design techniques.
2. To develop design and implementation skills of combinational and sequentiallogic circuits.
3. To introduce digital logic design software such as VHDL Programming.

Course Outcomes :

1. Spectacle an awareness and apply knowledge of number systems, codes, Boolean algebra and use necessary A.C, D.C Loading characteristics as well as functioning while designing with logic gates.
2. Use logic function representation for simplification with K-Maps and analyze as well as design Combinational logic circuits using SSI & MSI chips.
3. Analyze Sequential circuits like Flip-Flops (Truth Table, Excitation table), their conversion & design the applications.
4. Identify the Digital Circuits, Input/Outputs to replace by FPGA
5. Use VHDL programming technique with different modeling styles for any digital circuits.

Course Contents

UNIT – I NUMBER SYSTEM AND LOGIC FAMILIES 8 Hours

Introduction to digital electronics & Boolean algebra.
Number Systems - Binary, Octal, Hexadecimal and their conversions.
Signed Binary number representation and Arithmetic's: Signed & True Magnitude, 1's complement, 2's complement representation and arithmetic's.
Codes: BCD, Excess-3, Gray code, Binary Code and their conversion.
Switching characteristics of BJT & FET, IC Characteristics.
TTL: Standard TTL characteristics, Operation of TTL NAND gate, Subfamilies, Configurations-Active pull-up, Wired AND, totem pole, open collector.
CMOS: Standard CMOS characteristics, operation of CMOS NAND, Subfamilies, CMOS configurations Wired Logic, Open drain outputs.
Comparison of TTL & CMOS, Interfacing: TTL to CMOS and CMOS to TTL

UNIT – II COMBINATIONAL LOGIC DESIGN 8 Hours

Logic minimization: Representation of truth-table, SOP form, POS form, Simplification of logical functions, Minimization of SOP and POS forms, don't care Conditions.
Reduction techniques: K-Maps up to 4 variables and Quine - McClusky technique.
CLC design using SSI chips – Code converters, Half- Adder, Full Adder, Half Subtractor, Full Subtractor, n bit Binary adder, Look ahead carry generator.Magnitude comparator using IC 7485.
Introduction to MSI functions & chips - Multiplexers (IC 74151 and IC 74153), Decoder / Demultiplexer (IC 74138), Encoder (IC 74147), Binary adder (IC 7483).

CLC design using MSI chips – BCD & Excess 3 adder & subtractor using IC 7483, Implementation of logic functions using IC 74151,74153& 74138.

UNIT – III SEQUENTIAL LOGIC **8 Hours**

Introduction to sequential circuits. Difference between combinational circuits and sequential circuits, memory element – latch.

Flip- Flops: Design, truth table, excitation table of SR, JK, D, T flip flops. Study of flip flops with asynchronous and synchronous Preset & Clear, Master Slave configuration, conversion from one type to another type of flip flop. Study of flip flop ICs - 7473, 7474, 7476.

Application of flip-flops – Bounce elimination switch, Counters- asynchronous, synchronous and modulo counters study of modulus n counter ICs- 7490, 74191 & their applications to implement mod counters.

UNIT – IV SEQUENTIAL LOGIC DESIGN **8 Hours**

Registers- Buffer register, shift register types - SISO, SIPO, PISO & PIPO, applications of shift registers - ring counter, twisted ring counter, study of universal shift register IC – 74194,

Sequence generators using counters & shift register, Pseudo Random Binary Sequence Generator.

Basic design steps-State diagram, State table, State reduction, State assignment, Mealy and Moore machines representation, Implementation, finite state machine implementation, sequence detector using Moore & Mealy model.

UNIT – V PROGRAMMABLE LOGIC DEVICES AND INTRIDUCTION TO HDL **6 Hours**

Algorithmic State Machines- ASM notations, charts (eg- counters, washing machine, lift controller, vending machine), design using multiplexer controller method (eg- counters).

Introduction to PLD's – ROM, PAL, PLA, Design of 4 variable SOP using PLDs, Basic architecture of SPLD and CPLD, Study of CPLD architecture XC9572, Basic architecture of FPGA, CPLD. Design flow (Basic Concept of Simulation and Synthesis)

Introduction to HDL – Necessity, Characteristics & Types.

UNIT - VI VHDL PROGRAMMING **6 Hours**

Introduction to VHDL - Library, Package, Entity, Architecture, Data Objects (Variable, signal & constant), Data Types (scalar, composite array type & predefined data types, Attributes (necessity and use. 'event attribute). **VHDL Modeling styles –** Dataflow, behavioral & structural

VHDL statements - Concurrent Statements (With. Select, When..Else), Sequential Statements (if..else, case)

VHDL design Examples - Multiplexer, binary adder, counter, shift register.

Text Books

1. "Modern Digital Electronics ", R.P. Jain, 3rd Edition, Tata McGraw-Hill, ISBN: 0–07–049492–4
2. "Fundamentals of Digital Logic with VHDL Design", Stephen Brown, ZvonkoVranesic McGraw-Hill, ISBN: 978–0–07–352953–0

Reference Books

1. "Digital Principles", Flyod, Pearson EducationISBN:978-81- 7758-643-6.
2. "Digital Design", M Morris Mano, Prentice Hall, 3rd Edition, ISBN: 0130621218.
3. "Digital Logic applications and Design", John Yarbrough, Thomson Publication ISBN: 978-0314066756
4. "Digital Principles and Applications", Malvino, D. Leach, 5th edition, Tata McGraw Hill
5. "VHDL Primer", J.Bhaskar, Pearson Education,3rd Edition, ISBN: 0071226249
6. "Switching and Finite Automata Theory", Kohavi Z., Jha N.K,, Cambridge University Press, India, 2nd Edition, ISBN: 978-0-521-85748-2